## ABSTRACT OF THE DISCLOSURE

A mobile station includes an RF transceiver and a user interface. The mobile station further includes a plurality of data processor cores each having a first interface supporting a first bus coupled to an associated one of a plurality of program memories, a second interface supporting a second bus coupled to a common data memory, and a third interface supporting a third bus coupled to at least one input/output device. Each of the first, second and third buses include an address bus that is sourced from the processor core and a data bus. The plurality of data processor cores may be contained within a single integrated circuit package, such as an ASIC, in a System on Chip (SoC) configuration. In this case a first processor core may function as a CPU for controlling the overall operation of the mobile station, including the user interface, while a second processor core functions as a DSP for controlling operation of the RF transceiver. The first interface supports a unidirectional data bus from the program memory, and the second interface and the third interface each support a bidirectional data bus. Each of the plurality of processor cores has the second interface coupled to the common data memory through a common memory control unit, and the third interface is coupled to at least one of a plurality of interface devices through a common control bus unit. Each of the processor cores operates with a clock signal and fetches an instruction from the associated one of the plurality of program memories using the address bus and the data bus of the first interface, the instruction fetch being referenced to a predetermined edge of the clock signal. Each processor core then begins an execution of the fetched instruction on a next occurrence of said predetermined edge of said clock signal. The first interface is responsive to an assertion of a HOLD signal for suspending the fetching of a next instruction from the program memory. The segregation of the program, data and control buses provides for increased efficiencies and bus bandwidth, increasing the number of instructions that are executed per unit of time at a given clock frequency.